In the Claims

In accordance with 37 C.F.R. § 1.121(c)(1)(i) and (c)(3), the following is a clean version of the pending claims incorporating the newly introduced amendments. In accordance with 37 C.F.R. § 1.121(c)(1)(ii), Attachment A provides marked-up versions of the amended claims illustrating the newly introduced changes to those claims.

1. (Amended) A computer system comprising:

a first processor;

a transmission line coupled to the first processor;

a monitor including a receiver input gate coupled to the transmission line; and

changing circuitry

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coupled to the transmission line and to the receiver input gate and

capable of changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of the receiver input gate, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the change is made.

2. (Amended) The computer system of claim 1, wherein:

a software program coupled to a second processor enables a user of the computer system to initiate the changing at least one of the pedestal voltage level and the signal threshold voltage level.

3. The computer system of claim 2, wherein:

the software program provides an on-screen display capability.

4. (Amended) The computer system of claim 1, further comprising:
a synchronization processor coupled to the receiver input gate; and
monitoring circuitry
coupled to the synchronization processor and
capable of
monitoring an output of the synchronization processor and
detecting irregularly timed synchronization processor output signals; and
wherein the changing circuitry is further capable of changing at least one of the pedestal voltage level and the signal threshold voltage level when the monitoring circuitry detects irregularly timed output signals.

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5. (Amended) The computer system of claim 4, wherein:
the changing is initiated by a software program coupled to a third processor.

6. (Amended) The computer system of claim 4, wherein:
the detecting includes comparing output of the synchronization processor to a stable time reference.

7. (Amended) The computer system of claim 4, wherein:
the detecting includes comparing output of the synchronization processor to phasing of an output of a video amplifier.

8. (Amended) The computer system of claim 1, wherein:
the transmission line carries horizontal synchronization signals.

9. The computer system of claim 1, wherein:
at least one of the pedestal voltage level and the signal threshold voltage level is raised.

10. The computer system of claim 1, wherein:
at least one of the pedestal voltage level and the signal threshold voltage level is lowered.

11. The computer system of claim 1, wherein:

at least one of the pedestal voltage level and the signal threshold voltage level is changed by a predetermined amount.

12. The computer system of claim 11, wherein:

the predetermined amount is approximately 100 mV.

13. The computer system of claim 1, wherein:

the pedestal voltage level is changed.

14. The computer system of claim 13, wherein:

the pedestal voltage level is changed by changing the potential of a point between the receiver input gate and an impedance approximating the characteristic impedance of the transmission line, wherein the approximating impedance is connected to ground.

15. The computer system of claim 1, wherein:

the signal threshold voltage level is changed.

16. The computer system of claim 15, wherein:

the signal threshold voltage level is changed by changing a reference voltage of the receiver input gate at a monitor end of the transmission line.

17. A method of reducing an effect of signal distortion from reflection on a transmission line, comprising:

changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of a receiver input gate coupled to the transmission line, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the changing, and such that the effect of signal distortion from reflection on the transmission line is reduced.

18. (Amended) The method of claim 17, further comprising:

detecting the effect of signal distortion from reflection on the transmission line caused by a substantial equality of the pedestal voltage level and the signal threshold voltage level.

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19. (Amended) The method of claim 17, wherein:

the changing includes using a software program coupled to a first processor to initiate the changing.

20. The method of claim 19, wherein:

the software program provides an on-screen display capability.

21. (Amended) The method of claim 17 wherein:

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the transmission line is contained in an interface cable connecting

a second processor coupled to a memory; and

the second processor contains the signal threshold voltage level.

22. The method of claim 21, wherein:

the transmission line carries horizontal synchronization signals.

23. The method of claim 17, wherein:

the changing includes raising at least one of the pedestal voltage level and the signal threshold voltage level.

24. The method of claim 17, wherein:

the changing includes lowering at least one of the pedestal voltage level and the signal threshold voltage level.

25. The method of claim 17, wherein:

the changing includes changing at least one of the pedestal voltage level and the signal threshold voltage level by a predetermined amount.

26. The method of claim 25, wherein:
the predetermined amount is approximately 100 mV.

27. The method of claim 17, wherein:
the pedestal voltage level is changed.

28. The method of claim 27, wherein:
the pedestal voltage level is changed by changing the potential of a point between the receiver input gate and an impedance approximating the characteristic impedance of the transmission line, wherein the approximating impedance is connected to ground.

29. The method of claim 17, wherein:
the signal threshold voltage level is changed.

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30. (Amended) The method of claim 29, wherein:
the signal threshold voltage level is changed by changing a reference voltage of the receiver input gate at an end of the transmission line that is coupled to a monitor.

31. The method of claim 17, wherein:
the detecting includes monitoring an output of a synchronization processor for irregularly timed output signals.

32. The method of claim 31, wherein:
the changing is initiated by a software program when the monitoring detects irregularly timed output signals.

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33. (Amended) The method of claim 31, wherein:
the detecting includes monitoring an output of the synchronization processor for irregularly timed output signals by comparison to a stable time reference.

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34. (Amended) The method of claim 31, wherein:

the detecting includes monitoring an output of the synchronization processor for irregularly timed output signals by comparison to phasing of an output of a video amplifier.

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35. An apparatus for reducing an effect of signal distortion from reflection on a transmission line, comprising:

means for changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of a receiver input gate coupled to the transmission line, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the changing, and such that the effect of signal distortion from reflection on the transmission line is reduced.

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36. (Amended) The method of claim 35, further comprising:

means for detecting the effect of signal distortion from reflection on the transmission line caused by a substantial equality of the pedestal voltage level and the signal threshold voltage level.
